

GDQN

LVDS
Differential

0.6 ps
RMS Jitter

SMD

2.5 V

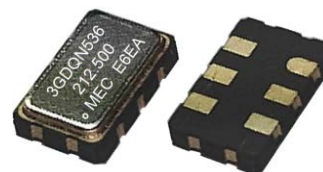
3.3 V

Min.
10 MHz

Max.
1,500 MHz

Features

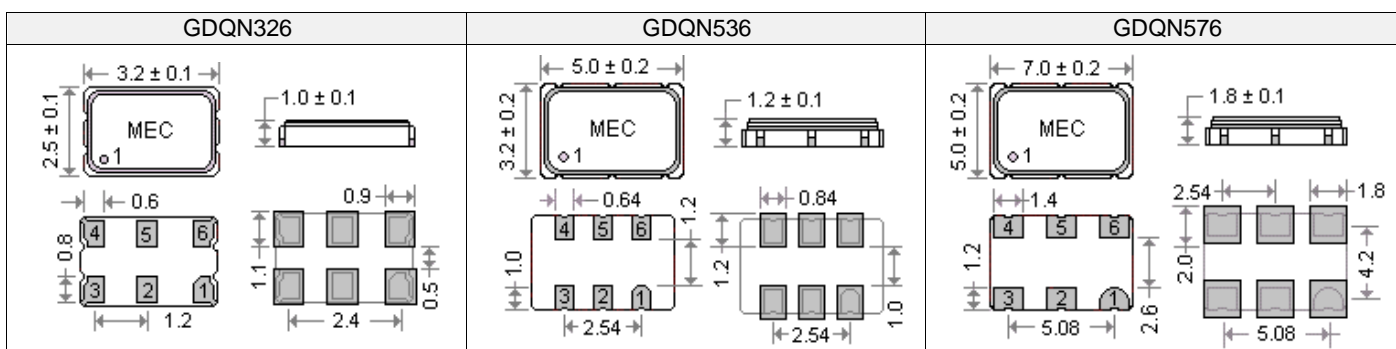
Mercury's Low Jitter Differential VCXO, with low current consumption (22 mA for LVDS 622.080 MHz at 3.3V) & an integrated phase jitter performance of 0.6pS RMS. Gaining its precision frequency control market position by providing engineers with *few days* samples for prototypes and low cost, fast delivery for volume production. The perfect solution to replace traditional XO's & VCXO's that use a more expensive high-frequency, fundamental crystal and a noisy PLL multiplier circuit.



General specifications , at Ta=+25°C

Model	GDQN									
Available Frequency Range	10 ~ 1,500 MHz									
Supply Voltage V _{DD} (code)	+ 2.5 V _{DD} ± 5 % (voltage code ' 25 ')					+ 3.3 V _{DD} ± 5 % (voltage code ' 33 ')				
Current with Output Disable	16 mA typical									
Current Consumption (V _{DD} = +2.5 V)	100 MHz : 16 mA	250 MHz : 18 mA	500 MHz : 21 mA	750 MHz : 22 mA	1,000 MHz : 24 mA	1,350 MHz : 26 mA				
Current Consumption (V _{DD} = +3.3 V)	100 MHz : 25 mA	250 MHz : 30 mA	500 MHz : 35 mA	750 MHz : 39 mA	1,000 MHz : 43 mA	1,350 MHz : 47 mA				
Frequency Stability Codes	Frequency Stability over Operating Temperature Range		± 25 ppm	± 50 ppm	± 100 ppm	If non-standard , please enter the desired stability after the " C " or " I " represents . For example : " C20 " ± 20 ppm over -10°C to +70°C ; " I20 " ± 20 ppm over -40°C to +85°C				
	Commercial (-10°C to +70°C)		A	B	C					
	Industrial (-40°C to +85°C)		D	E	F					
Output Logic " High " , " 1 "	1.4 V typical ; 1.6 V max.			Output Logic " Low " , " 0 "			0.9 V min. ; 1.1 V typical.			
Load	100 Ω between output and complimentary output			Rise Time / Fall Time			0.4 ns. (max.) [20% ↔ 80% waveform]			
Duty Cycle	50 % ± 5%			Aging at Ta = +25°C			± 5 ppm max. for first year at 25°C			
Start-up Time	10 m sec. (max.)			Storage Temperature			-55°C to + 150°C			
SSB Phase Noise [dBc / Hz (typical)]	Offset	77.76	122.88	125	156.25	212.5	491.52	622.08	1000	1250
	10 Hz	-74	-68	-69	-67	-53	-56	-51	-46	-32
	100 Hz	-104	-98	-97	-92	-86	-87	-77	-80	-68
	1 KHz	-121	-114	-114	-112	-109	-101	-99	-96	-94
	10 KHz	-130	-123	-124	-121	-118	-110	-109	-105	-103
	100 KHz	-134	-127	-129	-124	-121	-113	-114	-108	-105
	1 MHz	-140	-138	-136	-136	-133	-125	-121	-116	-117
10 MHz	-157	-155	-154	-153	-151	-143	-141	-135	-136	
Phase Jitter (12KHz ~ 20 MHz, RMS) unit : ps.	0.5	0.6	0.5	0.6	0.6	0.6	0.5	0.7	0.6	
Control Voltage Function on Pad 1										
Supply Voltage (V _{DD})	V _{DD} = +2.5 V ; Vcon Center = +1.25V					V _{DD} = +3.3 V ; Vcon Center = +1.65V				
Vcontrol Range	+ 0.2V ~ +2.3V ± 80 ppm (min.)					+ 0.3V ~ +3.0V ± 80 ppm (min.)				
Frequency Pulling Range	Up to ± 200 ppm (min.) is also available. Please contact Mercury.									
Absolute Voltage	2.8 V max. for 2.5V V _{DD} ; 4.0 V max. for 3.3V V _{DD}									
Linearity	± 5% typical. ±10% (max.)			Input Impedance			1 MΩ typical			
Transfer Function	Positive Transfer			Bandwidth			10 KHz min. Measured at -3 dB			
Output Enable Function										
OE Control on Pad 2	70% of V _{DD} (min.) to enable output. (Open connection prohibit) 30% of V _{DD} (max.) to disable output.									
Output Enable Time / Disable Time	200 ns. Max. / 50 ns. Max.									

Outline Dimensions (Unit : mm) , Suggested pad Layout for SMDs



Pad Connections

Pad 1 : VCXO ; Pad 2 : OE: High Enable ; Pad 3 : Ground
Pad 4 : Differential ; Pad 5 : Complementary ; Pad 6 : Supply Voltage

GTQN	GPQN	GDQN	Q family	SMD	2.5 V	3.3 V
CMOS waveform	PECL Differential	LVDS Differential	N series			

Part Number Format and Example

Example : 3GPQN576 - E - 100N - 622.080

3	GPQN	576	-	E	-	100N	-	622.08
Supply Voltage	GTQN : CMOS	Package Size	Frequency Stability Code " E " :			±100 ppm (min.)		Frequency
" 3 " for 3.3V	GPQN : PECL	" 576 " : 7x5 mm	± 50 ppm over -40 to +85°C			frequency pulling range		(MHz)
" 25 " for 2.5V	GDQN : LVDS	" 536 " : 5x3.2 mm	Other frequency stabilities are available.					

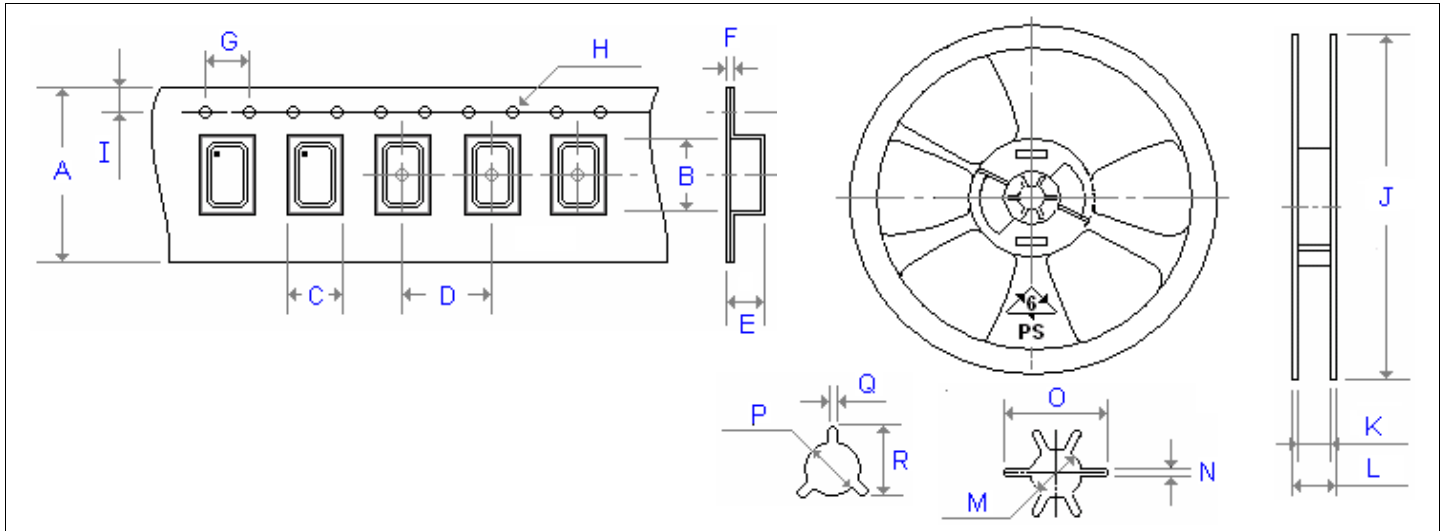
Test Circuits and Output Waveforms

CMOS Test Circuit	PECL Test Circuit	LVDS Test Circuit
	<p style="text-align: center;"> $V_{DD} = 3.3V; R1 = R3 = 127 \Omega; R2 = R4 = 82.5 \Omega$ $V_{DD} = 2.5V; R1 = R3 = 250 \Omega; R2 = R4 = 62.5 \Omega$ </p>	
CMOS Output Wave Form	PECL Output Wave Form	LVDS Output Wave Form

Emboss Taping and Reel Specifications

[VCXO]

[(VC)TCXO]



Carrier Type Dimensions (unit : mm)

	A	B	C	D	E	F	G	H	I	pcs / reel
G_324 (6)	8.0	3.4	2.7	4.0	1.4	0.3	4.0	∅ 1.50	1.75	3000
G_534	12.0	5.3	3.6	8.0	1.4	0.3	4.0	∅ 1.55	1.75	1000
G_576	16.0	7.3	5.3	8.0	1.9	0.3	4.0	∅ 1.55	1.75	1000
G_42	24.0	12.4	10.3	16.0	5.0	0.3	4.0	∅ 1.55	1.75	500
G_43	24.0	12.4	10.3	16.0	5.0	0.3	4.0	∅ 1.55	1.75	500
G_62	24.0	12.4	10.3	16.0	5.0	0.3	4.0	∅ 1.55	1.75	500
G_63	24.0	12.4	10.3	16.0	5.0	0.3	4.0	∅ 1.55	1.75	500
(V)M_22	8.0	2.8	2.3	4.0	1.1	0.3	4.0	∅ 1.50	1.75	3000
(V)M_32	8.0	3.4	2.7	4.0	1.4	0.3	4.0	∅ 1.50	1.75	3000
(V)MQ_326	12.0	3.6	2.9	4.0	1.7	0.3	4.0	∅ 1.55	1.75	3000
(V)M_53	12.0	5.3	3.6	8.0	1.4	0.3	4.0	∅ 1.55	1.75	1000
(V)M_57	16.0	7.4	5.5	8.0	2.8	0.4	4.0	∅ 1.50	1.75	500
(V)M_42	24.0	12.4	10.3	16.0	5.0	0.3	4.0	∅ 1.55	1.75	500
(V)M_43	24.0	12.4	10.3	16.0	5.0	0.3	4.0	∅ 1.55	1.75	500
(V)M_62	24.0	12.4	10.3	16.0	5.0	0.3	4.0	∅ 1.55	1.75	500
(V)M_63	24.0	12.4	10.3	16.0	5.0	0.3	4.0	∅ 1.55	1.75	500

Reel Dimensions (unit : mm)

	J	K	L	P	Q	R	pcs / reel
G_324 (6)	180.0	9.0	12.0	13.2	2.1	-	3000
G_534	180.0	13.0	16.0	13.2	2.5	-	1000
G_576	180.0	17.2	19.3	13.3	2.2	22.0	1000
G_42	330.0	30.0	25.0	13.4	2.5	19.5	500
G_43	330.0	30.0	25.0	13.4	2.5	19.5	500
G_62	330.0	30.0	25.0	13.4	2.5	19.5	500
G_63	330.0	30.0	25.0	13.4	2.5	19.5	500
(V)M_22	180.0	9.0	12.0	13.2	2.1	-	3000
(V)M_32	180.0	9.0	12.0	13.2	2.1	-	3000
(V)MQ_326	180.0	9.0	12.0	13.2	2.1	-	3000
(V)M_53	180.0	13.0	16.0	13.2	2.5	19.5	1000
(V)M_57	180.0	17.2	19.3	13.3	2.2	22.0	500
(V)M_42	330.0	30.0	25.0	13.4	2.5	19.5	500
(V)M_43	330.0	30.0	25.0	13.4	2.5	19.5	500
(V)M_62	330.0	30.0	25.0	13.4	2.5	19.5	500
(V)M_63	330.0	30.0	25.0	13.4	2.5	19.5	500

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